Sub-1V CMOS Bandgap Reference for Ultra-Low Power Applications

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Submitted in Partial fulfilment of the requirements
for the degree of M.Tech in VLSI and Embedded Engineering

Student's Declaration

I declare that the dissertation titled "Sub-1V CMOS Bandgap Reference for Ultra-Low Power Applications" submitted by Neha Dalal for the partial fulfilment of the requirements for the degree of Master of Technology in VLSI and Embedded Engineering is carried out by me under the guidance and supervision of Dr. M. S. Hashmi at Indraprastha Institute of Information Technology, Delhi and Mr. Vikas Rana at STMicroelectronics, Greater Noida. Due acknowledgements have been given in the report to all material used. This work has not been submitted anywhere else for the reward of any other degree.

..... Place and Date: .....

Neha Dalal

Certificate

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

…….
Dr. Mohammad. S. Hashmi

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Mr. Vikas Rana

Abstract

BCD silicon process technology is invented by ST which plays a pivotal role in today's industry. BCD is outcome of merging three different process technologies. The Digital, Analog and Power/High voltage elements are brought up on one single platform. This offers a unique range of voltage to cater large field of applications. Integration of best in class CMOS and HV devices is done which offers great link between design, technology and application.

Bandgap reference voltage generator is one of the critical blocks of the analog counterpart of a macro which is responsible for generating a PVT compensated voltage. The desensitized voltage is further used as the reference for many other blocks such is level shifters, voltage regulators. As we are scaling down the technology the supply voltage is also scaled down. So the conventional BGR are no longer applicable to meet the needs. Thus the bandgap reference in subthreshold region are utilized to meet the desired range of voltage of operation.

In this thesis, Bandgap Reference in subthreshold regime is designed using BCD9s (110nm) process technology. This is implemented to have applications in PCM/Flash memories designed in BCD technology at low supply voltages and in smart power applications. Two architecture are proposed:

The voltage mode BGR with the supply voltage of 950mV. It provides the reference voltage of 700mV, with a maximum coefficient of variation of 5% and temperature coefficient of 50ppm/^{o}C.

The current mode bandgap reference is designed with a supply voltage of 650mV, which generates a reference voltage of 250mV with a very low temperature variation of 35ppm/^{o}C. The static power consumption is 364nW at architecture level which is comparatively low which satisfies the ultra-low power applications.

Acknowledgement

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Firstly, I would like to thank my advisers Dr. Mohammad. S. Hashmi and Mr. Vikas Rana for providing excellent guidance and encouragement throughout the journey of this work. Without their guidance, this work would never have been a successful one. I also take this opportunity to express a deep sense of gratitude towards Design Engineer Ms. Preeti Mishra from SPT team at STMicroelectronics for her support and encouragement for conquering every hurdle that I have encountered throughout the process. I also like to thank Design Engineers Mr. Ritesh Mukherjee and Mr. Vivek Tyagi from SPT team, ST Microelectronics for the technical discussion whenever I was in need of any. My regards to all my friends at IIIT-D who made this journey a wonderful one. Last but not the least; I would like to thank my Parents for supporting me spiritually and emotionally.

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Chapter 1

Introduction

1.1 BCD

BCD (Bi-Polar-CMOS-DMOS), a single process platform is invented by STMicroelectronics in mid-eighties. With expertise in both “More-Moore” and “More-than-Moore” semiconductor technologies ST provides best class BCD solutions. It is a pivotal technology for power ICs. BCD is a superset of silicon processes, in which potency of three different process technologies is clubbed together. These three are, Bipolar for analog design, CMOS (Complementary Metal Oxide Semiconductor) for digital design and DMOS (Double diffused Metal Oxide Semiconductor) for power and high voltage devices. The benefits of bringing in all the three technologies are higher energy efficiency, improved reliability, reduced electromagnetic interference, smaller footprint hence reduced chip area, well power management. BCD is improving continually to address wide range of applications. A typical BCD product have key features of all three power, analog and digital. To tackle application specific needs, BCD offers optimized trade-off between performance, cost and functionality. BCD technology is continually innovating for better performance, introducing new technology modules, requires finer lithography for emerging memory solutions.

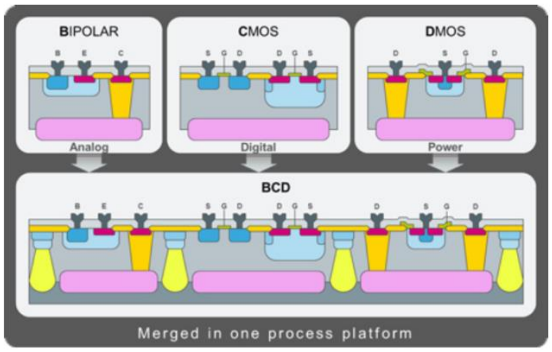

Figure 1 BCD Platform*

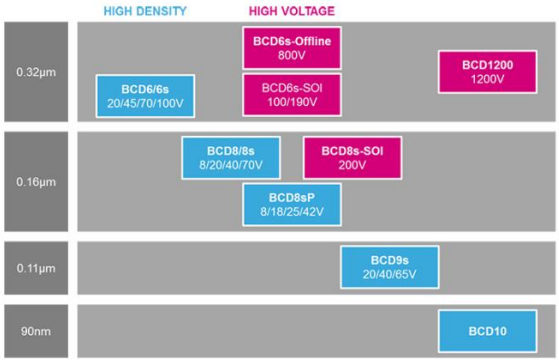

Figure 2 BCD Roadmap*

Broadly categorized in three domains:

1. Advanced BCD (BCD8s/8sP, BCD9s/sL, BCD10, BCD11)
2. SOI BCD (SOI-BCD6s, SOI-BCD8s, SOI-BCD9s)
3. High voltage BCD (BCD6s HV transformer)

Provides customized technology platform to reach optimal solution of the application. Various applications includes:

1. BCD for smart driving: engine management, airbag, vehicle electrification, car radio.
2. BCD for smart industry: motor control, lighting, bio-medical applications, displays.
3. BCD for smart houses and things: audio amplifiers, wireless charger, AMOLED display, Printers.

*Fig 1 and 2 have been taken from: https://www.st.com/content/st_com/en/about/innovation---technology/BCD.html

1.2 BGR Outline

The basic driving force behind the development of efficient and highly reliable BGR is the increased overall performance. Starting from the first conventional BGR in late seventies, BGR plays a pivotal role in designing integrated circuits. Nowadays highly precise and accurate references are in demand. BGR is a high performance block which have application in analog, digital, integrated systems, mixed signal. High resolution and high speed analog to digital convertors, digital to analog convertors, digital meters, servo systems, threshold detectors and many other control systems are some of the common applications.

BGR generates a precise reference, whether in a current mode or voltage mode, which is insensitive to process, temperature and voltage variations. These reference circuit should have sound static and dynamic performances. The static performance governs the accuracy of output reference voltage which can be improved by using methods like trimming. On the other hand the dynamic performance is affected by variations on devices temperature coefficient, channel length modulation, device mismatches, manufacturing and process variations, line regulation of reference. For references with utmost importance, temperature-compensated response is required. Well characterization of temperature- dependent components, voltages and currents is warranted to have accurate response. For precision in response the higher order temperature depended terms are utilized to compensate the undesired second-order effects.

With the advancement of CMOS technology low supply voltage becomes an important factor. So the conventional BGR, whose reference voltage is 1.2V typically, does not fit with the emerging submicron technologies (having supply voltage of 1.2V or less). Applications such as life- assist medical devices, wireless sensors have to work for long duration of time requiring very less supply voltage and operates with extremely low power dissipation.

1.3 Literature Review

In past recent years, many designs have been proposed in subthreshold which are PVT compensated. The following are some of them:

a. A 0.5V supply, 49nW Bandgap reference is designed in 40nm CMOS process [1]. The bandgap is enable using a 2X charge pump. The supply voltage of bandgap is generated by boosting the given 0.5V supply voltage two times using a charge pump. An optional duty cycle feature is also added to reduce the power consumption. To scale down the CTAT component diode connected MOS with degenerative resistors are used. With a supply voltage of 1V the temperature coefficient is 40ppm/^{o}C. Without trimming the temperature coefficient is 8ppm/^{o}C at 0.5Vsupply. This work offers five times less area with twice less power consumption at higher temperature compared to other designs at same technology and supply voltage.

b. A low voltage trimming free bandgap reference [2] is proposed which operates at 950mV supply voltage. The fabrication is done in 180nm CMOS triple technology. The design focus on minimizing the offset of the Opamp, which plays an important factor in causing variations in the reference output. An additional Opamp is used for this purpose instead of trimming resistors. It was proved that even with usage of 2 Opamp, the offset error is small. The coefficient of variation is 2.5%. The temperature coefficient for range of -45^{o}C-105^{o}C is 131ppm/^{o}C. The main drawback of the design is the power consumption that is 9.5uW.
c. A 32nW bandgap reference with a supply voltage of 0.5V [3] is proposed with a new architecture. This architecture utilized switched capacitor network, current controlled oscillator and a 2X charge pump. A similar approach is used as in [1], that the supply voltage is boosted up till 1V for bandgap core. The temperature stability is 75ppm/^{o}C for 0^{o}C to 80^{o}C. The design have significantly reduced the power consumption till 32nW. Without trimming the percentage variation of reference output voltage is about 2%. To reduce area, the concept of switched capacitor is used.
d. Another architecture is Sub-bandgap reference circuit for Nano watt LSIs [4]. In this paper both the bandgap and sub-bandgap are proposed in CMOS 180nm technology. The design includes only MOSFETs and Bipolar, no resistors are used. The current reference circuit which generates Nano amperes of current and PTAT voltage generator sources are used. BGR generate reference output of 1.09V with supply of 1.2V and sub-BGR generates 0.548V with the supply voltage of 0.7V. The coefficient of variation in both the BGR and Sub-BGR is 0.35% and 1.61% respectively. Additionally the temperature coefficient for temperature range of -40^{o}C to 120^{o}C is 147ppm/^{o}C and 114ppm/^{o}C for BGR and Sub-BGR respectively.
e. This design with a concept of reverse bandgap reference voltage is proposed [5] for ultra-low power applications. In this design the conventional diode connected PNP transistor is used along with a sampling scheme used for obtaining negative and positive temperature coefficients of reference voltages. This is done by using a clocked capacitor divider circuit. The reverse bandgap voltage is given as

$$V_{REF} = V_{BE}/\alpha + V_T \ln(N) \quad 1.1$$

Where the conventional bandgap reference voltage is given by

$$V_{REF} = V_{BE} + \alpha V_T \ln(N) \quad 1.2$$

With a supply voltage of 0.75V, a reference voltage of 250mV is obtained in CMOS 130nm technology. The temperature coefficient is 40ppm/^{o}C. The power consumption is also very less i.e. 170nW.

1.4 Thesis Organization

The thesis is organized as follows. Chapter 2 describes detailed working of Bandgap reference circuit. It also includes the effect of temperature, voltage and process over the reference voltage. Description of various blocks like operational amplifier, LDO, trimming circuit is also included. Finally chapter concludes with the exploration of various architecture of conventional Bandgap references.

Chapter 3 has detailed discussion on BGR operating in subthreshold regime. It presents subthreshold region of operation, various limiting factors of this region. Description of PVT compensating schemes utilized and also talks about the simulated results extracted across various process temperature and voltage.

Finally the Chapter 4 includes the conclusions by comparing the performance of proposed design with other designs and discuss about the future work for improving the scope in low power applications.

Chapter 2

Bandgap Reference

2.1 Principle of BGR

Bandgap reference is a core circuit on any chip which generates the exact reference. According to literature it does not have variations with respect to temperature, supply voltage fluctuation, process variations, or load current. The general approach of design of BGR is the addition of weighted sum of voltage which is increasing with temperature (PTAT) and the voltage which is decreasing with temperature (CTAT). The output of this summation is the compensated voltage w.r.t. temperature. This is called first order compensation with respect to temperature. For high precision reference voltages, the second order variations are cancelled by the quadratic temperature dependent parameters.

The voltage across diode is characterized with temperature, which is also stable with process variations. Thus all the precision reference circuits involve diodes (p-n junction) as the core, the design may vary slightly as the technology may differ but the techniques used are ultimately the same conceptually. In various designs, diode connected BJT and MOSFETs are used to serve the purpose of diode voltage. The first bandgap reference circuit is proposed by Robert Widlar, known as Widlar Bandgap reference whose output reference is equal to the bandgap voltage of silicon i.e. 1.23V at room temperature. This design is also called as conventional bandgap reference many a times.

2.1.1 Widlar Bandgap Reference

The idea behind the design is to compensate the PTAT (proportional to absolute temperature) and CTAT (complementary to absolute temperature) such that zero temperature coefficient is obtained. Mathematically it can be formulated as:

$$V_{ref}(T) = V_{PTAT} m_1(T) + V_{CTAT} m_2(T) \quad (2.1)$$

$$\frac{\partial V_{ref}}{\partial T} = m_1 \frac{\partial V_{PTAT}}{\partial T} + m_2 \frac{\partial V_{CTAT}}{\partial T} = 0 \quad (2.2)$$

Where m1 and m2 are the weights appended to get the appropriate sum so that $\frac{\partial V_{ref}}{\partial T}$ become zero. The term $\frac{\partial V_{PTAT}}{\partial T} > 0$ while the term $\frac{\partial V_{CTAT}}{\partial T} < 0$.

The V_{CTAT} term is obtained in circuit by using dioded connected BJT, V_{BE} of a BJT will yield CTAT component while the PTAT is formed by V_T, which in turn is result of ΔV_{BE} that is extracted from difference of V_{BE} which are having different current densities. The weighing factor M = $\frac{m_2}{m_1}$, is calculated by $\frac{\partial V_{ref}}{\partial T}$ = 0. The so obtained value is near zero temperature coefficient voltage. But this reference voltage is only first order

compensated , for higher order of compensation additional circuitary could be added. For implementation of the design shown in Fig.3 where diode connected NPN transistor, T1 is used to generate CTAT voltage. To generate ΔV_{be}, T2 with transistor ratio equal to 8 along with R1 is used. Operational amplifier is used to equalize the node Vin1 and Vin2. When Vin1 is equal to Vin2, then the voltage across R1 is the ΔV_{be}. The current through branch 1 and 2 is $\Delta V_{be}/R1$, where $\Delta V_{be} = VTln(N)/R1$. This PTAT current is mirrored to the branch 3, it is further converted into PTAT voltage by using R2 and added to the CTAT volatge.

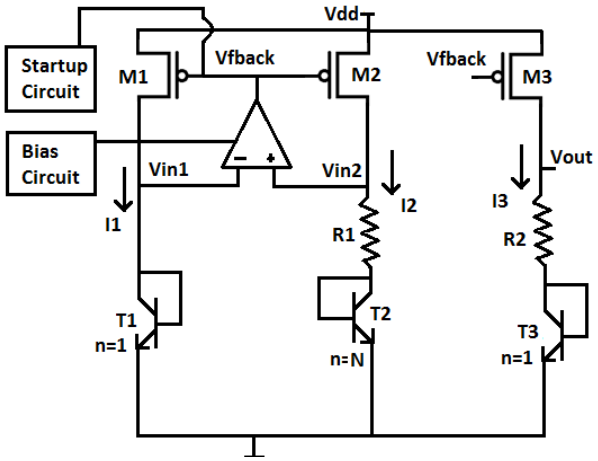

Figure 3 Conventional BGR core

2.2 PVT Variation

2.2.1 Temperature effect

a. Threshold voltage

The gate to source voltage required to invert the channel, or to accumulate enough charge carriers to form depletion region in channel.

$$V_{th} = V_{FB} + 2\Phi_F + \gamma\sqrt{2\Phi_F} \qquad 2.3$$

Where $\gamma = \sqrt{C_{ox} 2q\xi_{si} N_A}$.

The dependence of threshold voltage on temperature is found to be linear and is related as

$$V_{th}(T) = V_{th}(T_o) - \beta_{th}(T - T_o) \qquad 2.4$$

β_{th} is first order temperature coefficient and is given by differentiating V_{th} with respect to temperature. It is observed that threshold voltage decreases with temperature, i.e. have CTAT behavior.

b. Mobility

It is defined as the ratio of carrier velocity to the electric field, mobility decreases when the velocity of carriers starts to saturate. Dependence of mobility on temperature is given as

$$\mu_{n/p}(T) = \mu_{n/p}(T_o).(\frac{T_o}{T})^{\beta_{\mu n/p}} \quad 2.5$$

Where $T_o\ is$ absolute temperature. According to simulations it is observed that as the temperature increases the mobility decreases.

2.2.2 Process Variation

Process parameter variations can impact the performance of reference voltage. For minimizing the variations, the circuit is designed robustly to get minimized deviation across fast and slow corners. Generally the 3σ variations are quoted theoretically but the aim is to target better yield of fabricated circuit. To maximize the yield both process and local variations should be minimized. Matching of devices is one of the key considerations which needed to be taken care for MOSFETs. Various layout techniques are utilized to counteract the first order mismatch effects. Common centroid is one of the most used schemes, in which the two symmetric devices are placed about common center which helps in cancellation of any variations along x and y directions. Designing of Opamp and BGR core involve this consideration.

Another design consideration is to take resistor ratio in reference output so that process variations get cancelled. After fabrication, various trimming schemes are used to acquire the specific reference voltage. The trimming bits could be determined by parametric simulations across the extreme corners.

2.2.3 Voltage Variations

a. Line regulation

The variation of output reference voltage with respect to the variations in input voltage. The variation is quoted at room temperature. Mathematically line regulation is given by

$$\frac{\Delta V_{Ref}(\Delta V_{In})}{\Delta V_{In}}\ \mu V/V. \quad 2.6$$

$\Delta V_{Ref}(\Delta V_{In})$ Implies that the reference voltage is varied within a specific range of input voltage i.e. $\Delta V_{In}\ = V_{In,max} - V_{In,min}$, where $V_{In,min}$ denotes the minimum operating range of circuit and $V_{In,max}$ the maximum.

b. PSRR

At the time of practical implementation on silicon, the power rails could get affected by high frequency noise, spurious signals because of coupling of signals or power surge. So the ability of the circuit to suppress or reject the noise at a particular frequency on power rail to obtain a stable reference voltage is defined as PSRR. It is expressed in dB. Mathematically PSRR is given as

$$PSRR = 20log\frac{V_{Ref(ac)}}{V_{In(ac)}}dB \quad (2.7)$$

2.3 Blocks Involved

2.3.1 Operational Amplifier

Operational amplifier is used to equalize the drain voltages (V_{in1} = V_{in2}), virtually shortening the two nodes. The Opamp is configured to form an inverting amplifier topology. Both the Vin1 and Vin2 nodes of Opamp will try to track each other. Depending upon the difference in the input voltages of the Opamp the output is set. The output of Opamp given as

$$A_v(dB) = 20\log(\frac{V_{OUT}}{(V_{in1}-V_{in2})}) \quad (2.8)$$

The output value is used to bias the current mirror of BGR core. Some of the key parameters which are given utmost importance are DC gain, voltage headroom, PSRR, Input offset. High gain is desired to minimize the input offset error. Voltage headroom should be sufficient to satisfy the desired bias conditions of MOSFETs whether saturation, subthreshold saturation or linear. High PSRR will results in less noise effects on reference voltage.

2.3.2 Startup

As the circuit is having metastable states, which means the circuit can be stable in both the equilibrium and quasi-equilibrium state. Start-up is utilized to avoid the quasi-equilibrium condition which can occur just at the onset of circuit. Initially when zero current is there in the circuit the nodes V_{in1} and V_{in2} are equal to zero, V_{in1} = V_{in2}= 0. This situation does not allow the Opamp output to change and hence output is zero. Start-up circuit provides the initial excitation externally to bring circuit out of the quasi-equilibrium state. Once the circuit start working, it should be noted that the start-up should not affect the performance parameters, including the reference output voltage.

2.3.3 Current Mirror

The current mirror used serves the two purposes, first the mirroring action for Opamp and second acts as the current source for BGR core. For mirroring current from one branch to another exactly, it is desirable to keep the V_{DS} of both the mirroring element same, for this to happen Ron is kept large. Generally length of the MOS is increased to serve the purpose. In bandgap if the current is not mirrored exactly, the slight mismatch in the current can lead to variations in the reference voltage. For maximizing the R_{ON} cascoding current mirror architecture of the can be used in [6]. This also helps in improving the PSRR of the circuit but of subthreshold operation where the supply voltage is the constraint this scheme cannot be utilized.

2.3.4 Trimming Circuit

Trimming is an adjustment technique which is done post fabrication to calibrate the circuit. Generally due to process variations the actual reference value got deviated from its desired value. One of the reasons is input offset error in Opamp, which arise due to variations in manufacturing ambience. It is very important to get desired accurate voltage value for a bandgap circuit. Trimming circuit plays a pivotal role, along with that the key point is at which component trimming should be done. As there are many sources of error in the circuit which leads many options for trimming. For example trimming could be done at output resistor as shown in Fig.4, $R2_1$ and $R2_2$, at output stage current source ($M3_1$, $M3_2$) or at BGR core diode connected MOS or transistor($T2_1$,$T2_2$).

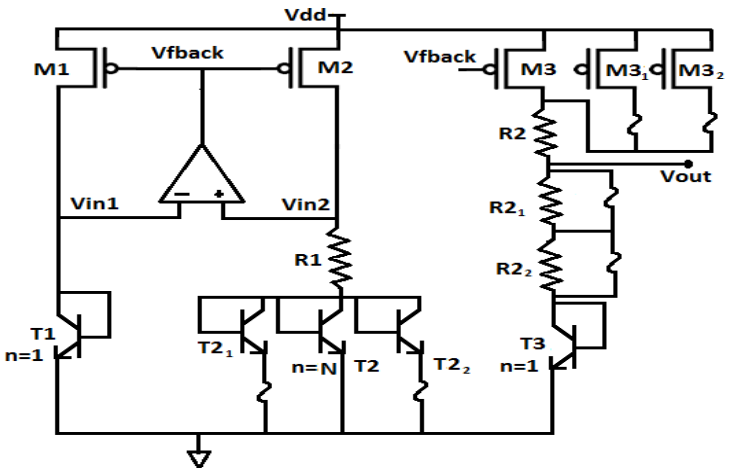

Figure 4 Current Trimming and Voltage trimming

There are two types of trimming, voltage trimming and current trimming. Resistor ladder trimming is for voltage trimming. Resistor ladder can be formed in a binary fashion to get desired step size. It is important to accurately analyze the desired voltages beforehand. A margin can be kept with the help of intermediate step voltages with calculated resistor values, it can be done by keeping step size small. While in

current trimming MOSFETs are used in parallel fashion. The length of the MOS is kept same and large for better mirroring. The width is varied according to the desired value of current which later with the help of resistor can be converted into desired voltage.

2.4 BGR Architectures

2.4.1 A 1.2V reference BJT Bandgap Reference Voltage Mode

The designed Bandgap is in voltage mode Fig. 5. The design specifications are as follows:

1. Supply voltage used is 1.8V
2. Simulated in BCD9s(110nm)
3. Two stage Opamp with PMOS input pair with external bias circuitry
4. R1 = 5KOhm, R_a=51.35KOhm , R_b= 2.5MOhm

It utilized NPN diode connected transistors to produce CTAT voltage (T1). The transistor ratio of T2 is kept 8, and R1, 5KOhm. The drop across R1 is $V_{be1} - V_{be2}$. By keeping the appropriate value of R1 and ΔV_{be}, the current of 8µA is fixed in branch 1 &2. Node Vin1 and Vin2 are equalized with the help of an Opamp. The ΔV_{be} is responsible for PTAT current generation. The current so generated is mirrored into the third branch and with the help of Ra the PTAT current is converted into PTAT voltage. By T3, the CTAT voltage is added to the PTAT voltage so generated. The One additional resistor, Rb with a value of 2.5MOhm, is used for provision of changing the CTAT slope at the output stage. The mathematical expression of the Vout node is given as:

$$V_{out} = \left(\frac{R_a}{R_1} V_T \ln(n) + V_{be}\right) \frac{R_b}{R_a + R_b} \qquad 2.9$$

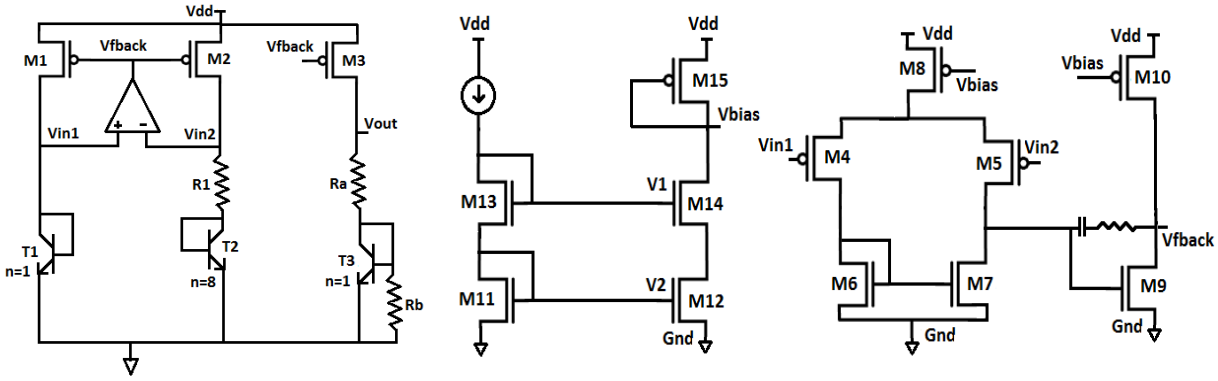

Figure 5 Voltage mode BGR core with OPAMP and Bias circuit

Two stage Opamp is used to equalize the node Vin1 and Vin2, the output of the Opamp, Vfback, is used to bias the current mirror of the BGR core. The offset error of Opamp is directly responsible for the variations in the reference voltage. So the gain of Opamp is kept sufficiently high to minimize the offset error. In design of an Opamp, PMOS are

used as input pair, just to satisfy the ICMR range. An additional circuitry is used for biasing of Opamp, which consumes 20uA.

The reference voltage is 1.2Vis generated, with a variation of 1.3mV across -40°C to 150°C. The current consumption is 65uA typically. At TYP Corner the DC simulation observed is shown below

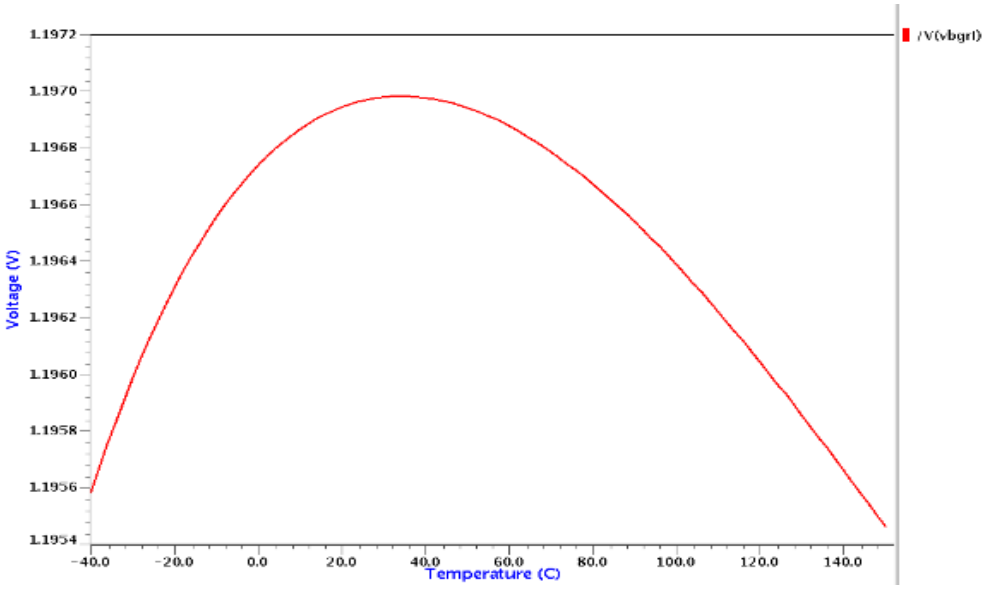

Figure 6 Vout variation across -40°C to 150°C

Table 1 Output voltage value and current consumption at all 3 corners for voltage mode BGR

Parameter/ corner	TYP	MIN	MAX
Current consumption	65µA	64.8µA	65.15µA
Vout	1.96V	1.207V	1.19V

2.4.2 A 1.8V BJT Bandgap Reference Current Mode

Another architecture of BGR Fig. 7, is explored which is in current mode. Design specifications are:

1. Supply voltage: 1.8V
2. Two stage Opamp with PMOS input pair with external bias circuitry
3. R1 = 5KOhm, R2,R3=48.2KOhm , R4= 23KOhm

This design is more robust in comparison to the architecture designed in 2.4.1 in terms of variations in reference voltage. Resistor R2 and R3 are responsible for CTAT Current slope while R1 is responsible for PTAT current slope. The weighted sum of PTAT and CTAT is finally mirrored to the third branch. R4 is responsible for the final voltage level of the reference. The advantage of current mode architecture is that, only with the

change in values of R2, R3 and R4 the desired voltage level with appropriate

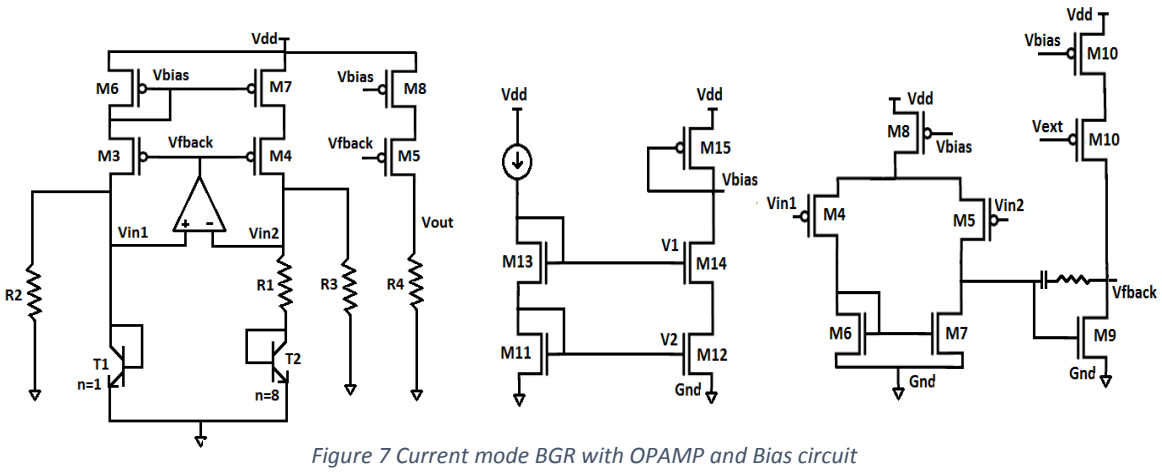

Figure 7 Current mode BGR with OPAMP and Bias circuit

compensation can be achieved. Cascoding is done in this design to enhance PSRR of the circuit.

Mathematically the reference output voltage is given as

$$V_{out} = (\frac{V_{be1}}{R_2} + \frac{\Delta V_{be}}{\mathrm{R_1}})\mathrm{R_4} \qquad 2.10$$

The DC variation at MIN corner across the temperature range of -40°C to 150°C is simulated. The curve is plotted below

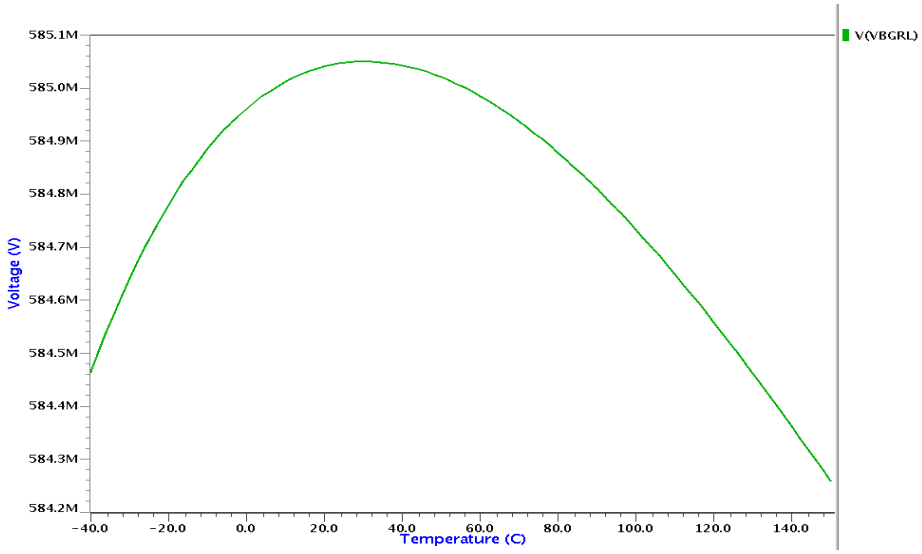

Figure 8 DC simulation of BGR output voltage over temperature

The generated reference voltage is 585mV. While the variations across the temperature is only 0.6mV, which is highly accurate. It is clearly observed that in current mode architecture the reference voltage can be set at any lower voltages depending upon the

value of R4. Thus this architecture is able to give a desired reference voltage the low power applications. Yet due to high supply voltage and additional external bias circuit of Opamp the circuit itself consumes high amount of current. To reduce the current consumption yet another architecture is explored.

Table 2 Output voltage value and current consumption at all 3 corners for current mode BGR

Parameter/ corner	TYP	MIN	MAX
Current consumption	118.5µA	150µA	97.7µA
Vout	585.1mV	598.1mV	578.24mV

2.4.3 Improved current mode BGR, without any additional external bias circuit

The architecture used is same as described in 2.4.2 i.e. the current mode design with cascoding. But in this design the external bias circuit is removed and BGR core is itself utilized to bias the Opamp, as shown in Fig. 9. The design specifications are:

1. Supply voltage: 1.8V
2. Two stage, PMOS input pair Opamp without external bias.
3. R1= 7.9KOhm, R2=R3= 75.2KOhm, R4= 36.9KOhm

In this design the BGR is responsible for the biasing of the Opamp. The Vbias voltage generated with the diode connected PMOS is used to bias the current mirror of the Opamp. The additional consumption of the current flowing through the external bias is saved in this design.

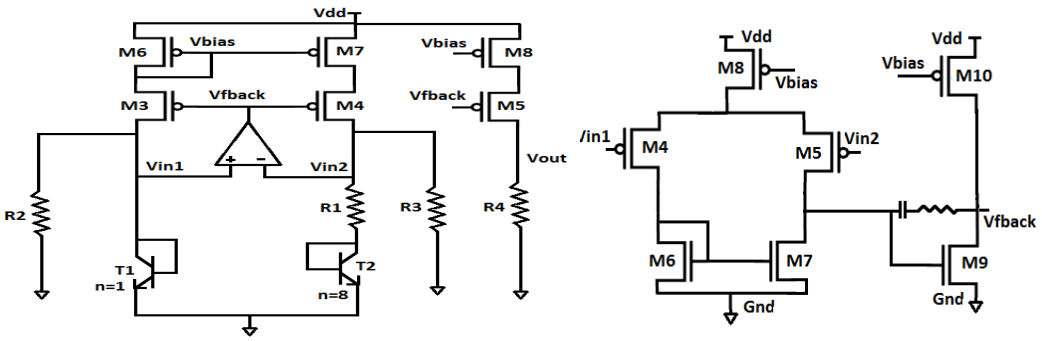

Figure 9 Current mode BGR with cascoding and self Bias OPAMP

The generated reference voltage is 600mV with a temperature variation of 1mV. At MIN corner the variation observed is maximum as compared to TYP and MAX corner. The DC simulated result is shown in Fig. 10

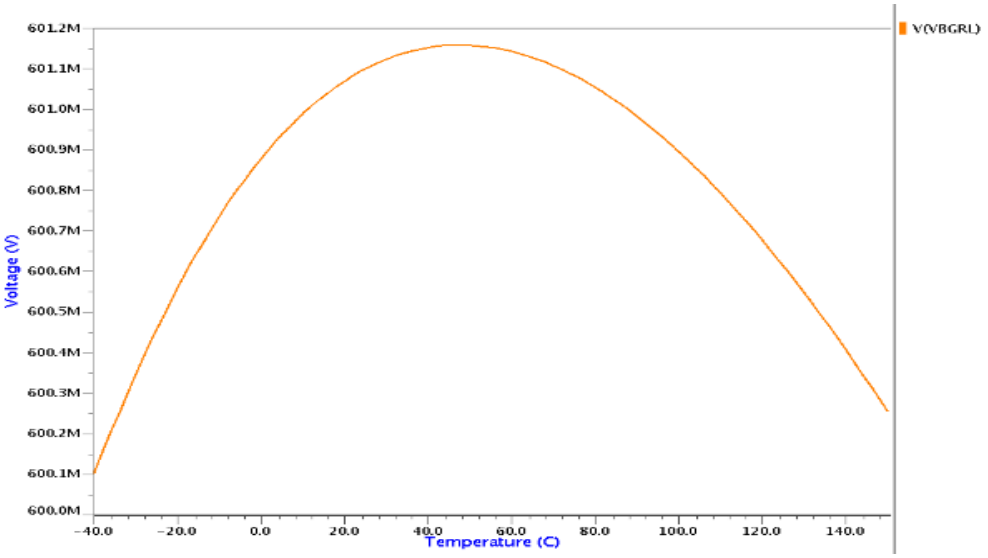

Figure 10 DC simulation of output of BGR over temperature

Table 3 Output voltage and current consumption at all 3 corners for improved current mode BGR

Parameter/ corner	TYP	MIN	MAX
Current consumption	54.2µA	76.2µA	30µA
Vout	592.1mV	600.1mV	586.4mV

2.4.4 BGR with MOS in subthreshold region

To have a design with MOS only, the current mode architecture is further explored. Instead of NPN transistor diode connected NMOS is used as shown in Fig 11. The key motivation to bias diode connected NMOS in subthreshold is the resemblance of the current equation in subthreshold region with the current equation of the diode connected NPN or PNP transistor. The current equation in subthreshold region is given as:

$$I_D = I_{DO}(\frac{W}{L})e^{\frac{V_{GS}}{nV_t}}(1 - e^{-V_{DS}/V_t}) \qquad 2.11$$

Also, as compared to NPN or PNP transistor the MOS will occupy less area. Additionally the voltage headroom can be decreased to much lower extent from 1.8V to as low as 650mV.In this design the specifications are:

1. Supply voltage: 1.2V
2. Two stage Opamp with no external bias
3. R1 =15.2KOhm , R2=R3=47.6KOhm , R4=36.9KOhm

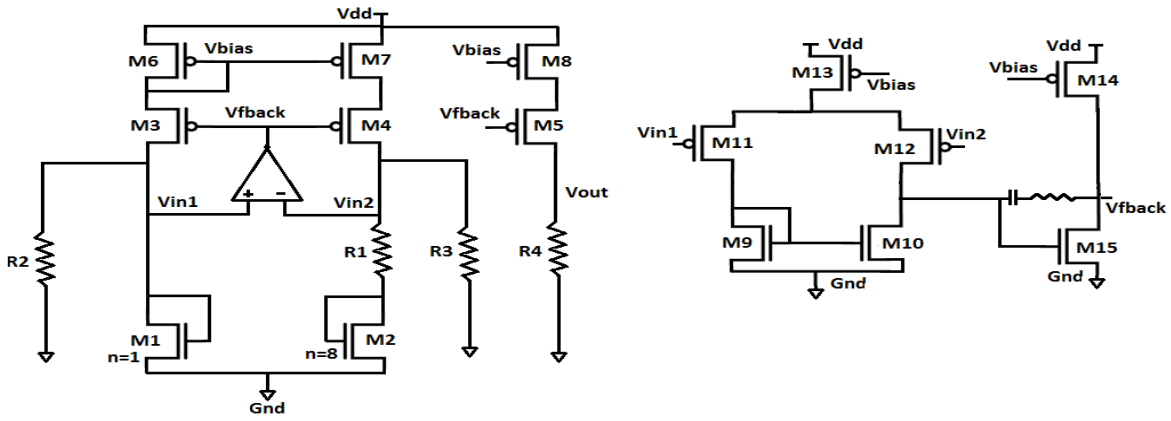

Figure 11 Current mode BGR with NMOS as core element

At TYP corner, the DC variation of V_{out} node over temperature range of -40°C to 150°C is plotted in Fig.12. the variation over temperature is 8mV.

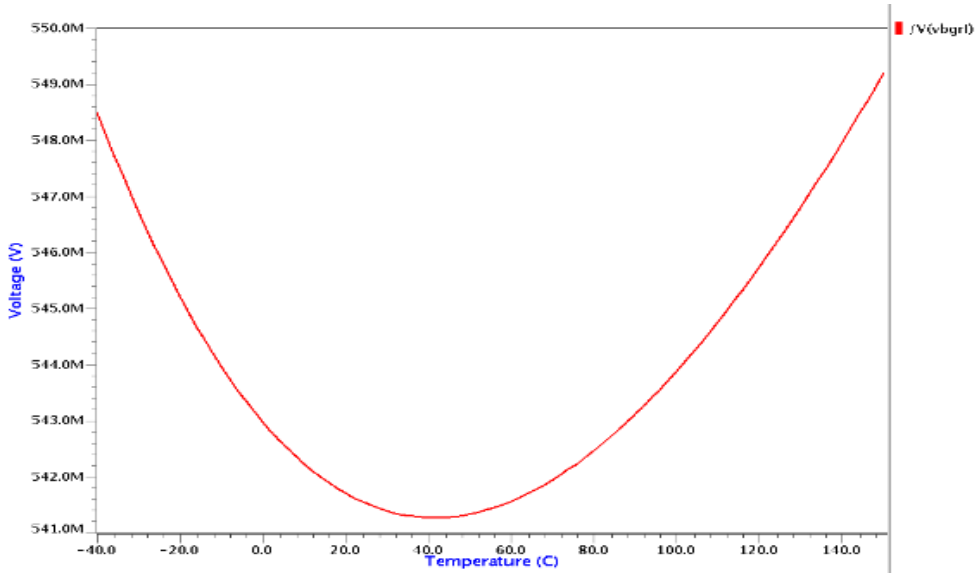

Figure 12 DC variation of Vout node of BGR

Table 4 Output voltage value and current consumption at all 3 corners for MOS Subthreshold BGR

Parameter/ corner	TYP	MIN	MAX
Current consumption	52.7µA	83.5µA	33.8µA
Vout	549mV	635.9mV	468mV

Although the variation in temperature is slightly greater as compared to the previous deigns, but the current consumption is almost comparable. With this idea and some modifications the final proposed design is very robust in terms of temperature variation.

Chapter 3

Design of BGR in Subthreshold Region

3.1 Subthreshold Region of Operation

According to the trend in IC fabrication the decrement in size tends to increase the speed and power consumption. Scaling down the size leads to increment in doping concentrations, this reduces breakdown voltage and increases electric field. To compensate for this supply voltage is lowered down. Working in Sub-1V means the supply voltage range is less than 1V and the reference output voltage which should be less than supply voltage, is much lower than 1V.

In general when V_{GS}=V_{TH}, the MOS starts to conducts, but it's not the actual scenario, $V_{GS} < V_{TH}$ there is some amount of drain current. This mode of operation is classified as subthreshold region and the drain current flowing in this regime is known as subthreshold current. In this region MOSFET is working in weak inversion region. In weak inversion region the carrier movement is modelled same that of BJT. The carrier first diffuse from source to bulk and then get collected at drain. To serve the low power applications, subthreshold region of operation is useful. But there are various challenges like low voltage headroom, mismatch, and noise.

The drain current is through I-V characteristics in subthreshold is expressed as

$$I_D = I_{DO}\left(\frac{W}{L}\right)e^{\frac{V_{GS}}{nV_t}}\left(1 - e^{-V_{DS}/V_t}\right) \quad 3.1$$

Where,

$$V_t = \frac{kT}{q} \approx 26\text{mV at T=300K} \quad 3.2$$

$$n = \frac{C_{ox} + C_{dep}}{C_{ox}} \quad 3.3$$

$$I_{DO} = \mu_n C_{ox}(n-1){V_t}^2 e^{-V_{TH}/nV_t} \quad 3.4$$

Saturation operation in subthreshold region occurs at V_{DS}>100mV. Keeping $V_{DS} > 4V_t$, where the drain current can be approximated as

$$I_D = I_{DO}\left(\frac{W}{L}\right)e^{\frac{V_{GS}}{nV_t}} \quad 3.5$$

$$I_D = \mu_n C_{ox}(n-1){V_t}^2\left(\frac{W}{L}\right)e^{\frac{V_{GS}-V_{TH}}{nV_t}} \quad 3.6$$

Drain current is having an exponential dependence on gate to source voltage.

Trans-conductance in subthreshold region is,

$$gm = \partial I_D / \partial V_{GS} \quad 3.7$$

$$gm = \frac{1}{nV_t} I_{DO} (\frac{W}{L}) e^{\frac{V_{GS}}{nV_t}} \quad 3.8$$

High gm/I_D corresponds to weak inversion region that is subthreshold region. As the current density reduces, the gm will attain a maximum value

$$gm = \approx \frac{I_d}{nV_t} \quad 3.9$$

3.2 Design Implementation

The conventional BGR have a reference output voltage of 1.2V approximately. But to support various low power application this reference voltage cannot be entertained. The proposed design illustrated in Fig. 13 and 16 utilizes the MOSFETs in Subthreshold regime, where gm is high which in turn improves current efficiency of circuit. The design is implemented in voltage mode, with supply voltage of 950mV. Another design is implemented for ultra-low power applications. The BGR is designed in current mode with the voltage of operation 600mV.

3.2.1 Design at 950mV supply voltage

In the core of BGR, the diode connected NMOS are responsible for CTAT voltage generation ($V_{GS,}$ M1 and M2 of 1st and 2nd Branch) and ΔV_{GS} generates the PTAT current which with the help of a resistor is converted into PTAT voltage (3rd stage). The 3rd stage does the addition of CTAT and PTAT voltages to get reference output voltage which is temperature compensated (V_{out}). The design considerations are:

a. Diode connected NMOS are kept in subthreshold. The size of these MOS are kept purposely large such that their threshold voltage is greater than the gate to source voltage. Also sufficient drain to source voltage is provided to keep MOS in well subthreshold saturation region of operation. These conditions are ensured by simulating the design over all the three process corners for complete range of temperature under consideration. Finally the design is optimized for all set of constraints to meet the bias margins.

b. The PMOS works as current source, as shown in Fig.13, the gate node of M4, M5, M6 are connected together to mirror the current in all the branches. Node Vfback is driven by the operational amplifier. The difference between the drain voltages of M1 and M2 serves as the input common mode range for operational amplifier.

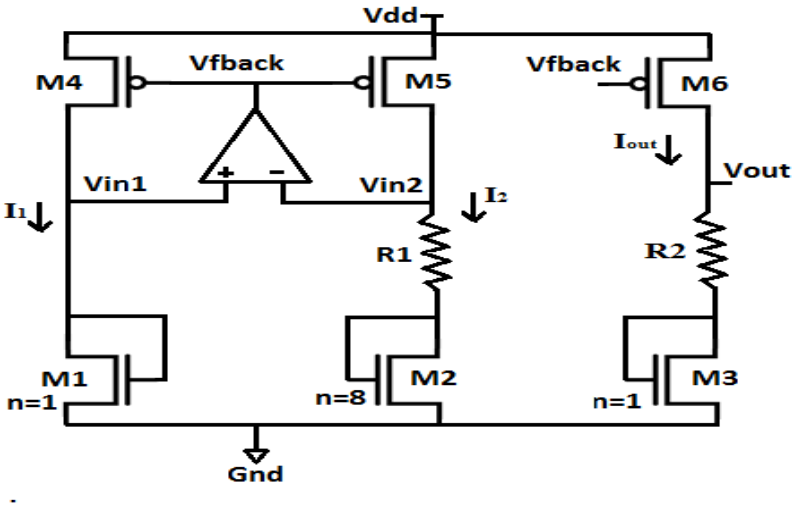

Figure 13 Voltage mode Architecture of BGR core

c. Operational Amplifier, as shown in Fig. 14, due to lower voltage headroom constraint the Opamp is designed such that input pair and mirror MOSFETs (M7, M8, M9, and M10) work in subthreshold saturation. While the M11 works in saturation region to provide constant current. The biasing of M11 is done by mirroring the V_{fback} node. M12~M16 are utilized to mirror and generate a bias voltage for M11. To let V_{bias} and V_{fback} node track each other M12~M16 are sized appropriately to satisfy the saturation margins.

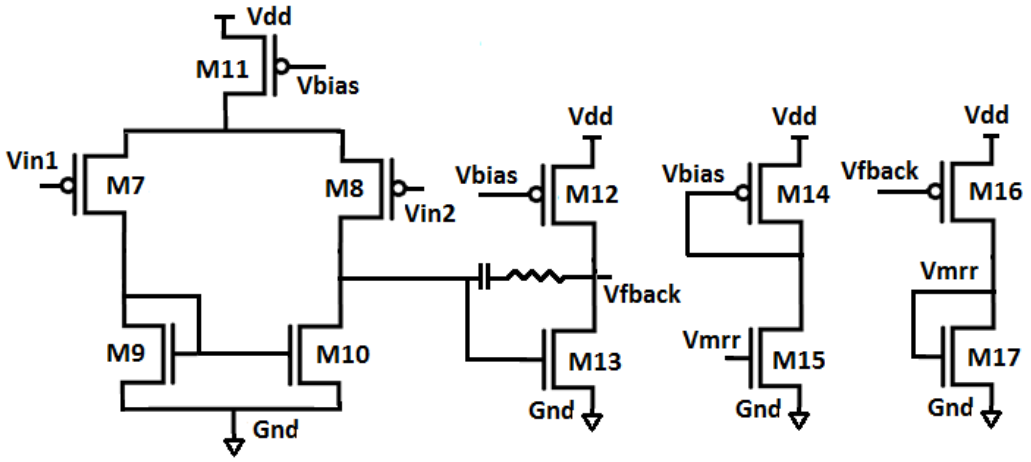

Figure 14 OPAMP design with Bias generating circuit

d. In startup, is designed such that it is electrically decoupled from the Bandgap core circuit while operating in equilibrium. The current injected into the circuit should not be so small that it takes lager time to charge the parasitic capacitance, this will unnecessarily increases the startup time.

A startup design with an inverter and a NMOS is implemented as shown in Fig.15. The V_{out} voltage is sensed by the invertor. Till the quasi-equilibrium state exists the V_{out} remains at low and thus driving the output of invertor as high. This in addition turns on the NMOS and Vfback node starts discharging as turning on of NMOS will tries to pull the Vfback node to ground. The Vfback is connected to the gate of current mirrors, thus lowering down of Vfback node potential will eventually startup the bandgap. As the Vfback node goes down the current source of BGR core starts to conduct the current in respective branches. To avoid the sudden transition of the V_{out} and Vfback nodes, capacitor is added at the output of inverter node. Value of the capacitor will determine the speed of the startup. The value should be chosen such that a sufficient time is available for the bandgap to settle at desired value.

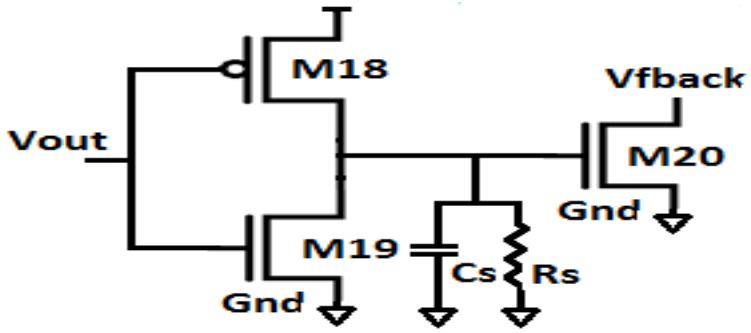

Figure 15 Startup Design

3.2.2 Design at 650mV supply voltage

The current mode architecture, as shown in Fig. 16, is implemented which produces a temperature independent voltage with the help of resistors. The core itself produces both the currents that are directly proportional to V_{GS} and ΔV_{GS}.

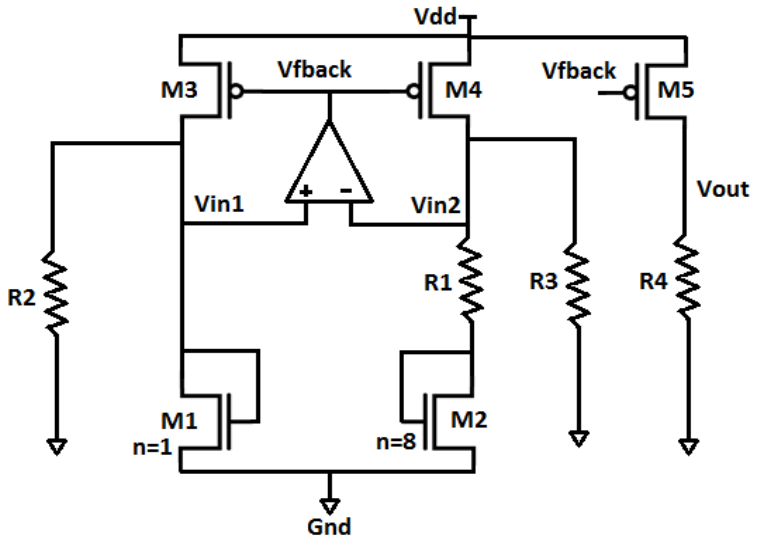

Figure 16 Proposed BGR core

a. The diode connected NMOS is sized such that the threshold voltage is always greater than the V_{GS} of NMOS. After simulations it was observed that as the channel length increases the threshold voltage increases also with increase in width the threshold voltage increases. Thus diode connected NMOS was simulated by applying a fixed current source of 60nA with variable as W and L. W and L were chosen such that V_{DS} is always greater than 4 V_T and V_T is greater than V_{GS}.

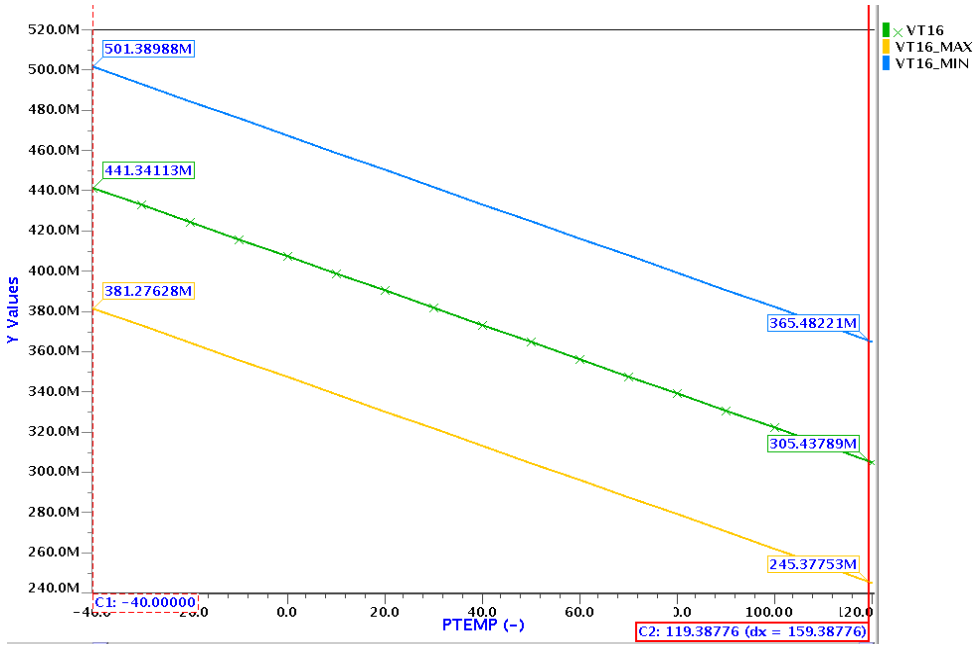

Figure 17 Vth variation across temperature for TYP, MIN and MAX corners of diode connected NMOS

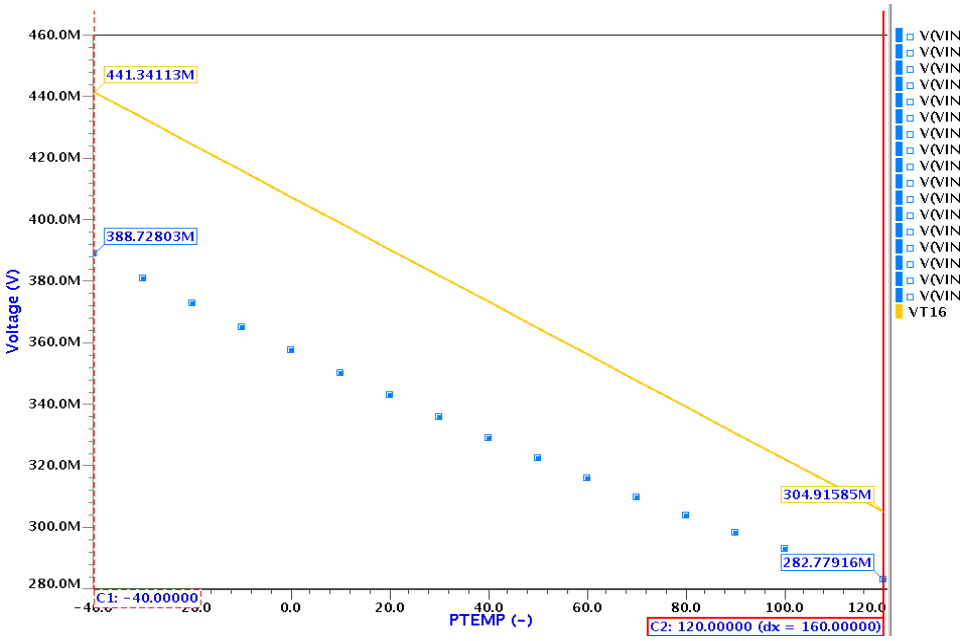

Figure 18 VGS voltage variation w.r.t threshold voltage of diode connected NMOS.

Fig. 17 shows the maximum to minimum range of V_{th} that is observed after simulation for MIN, TYP and MAX process corner over temperature sweep while Fig. 18 depicts the variation of V_{GS} and threshold voltage w.r.t. temperature of diode connected NMOS.

b. The PMOS current mirrors are kept of equal sizes such that equal amount of current flows through the branches, $I_1 = I_2 = I_3$. The sizing is done in such a way that proper V_{DS} is maintained across all the mirror PMOS and the desire gate voltage (V_{fback}) of them should not go below 100mV across any of the corner at any temperature. This is important to take care because Vfback is the output of single stage Opamp, thus Vfback node acts as drain node for one of the input pair of Opamp.
For proper work in subthreshold region the V_{DS} should always be maintained $>4V_T$, otherwise the V_{DS} effect in exponential form will be reflected in reference output.

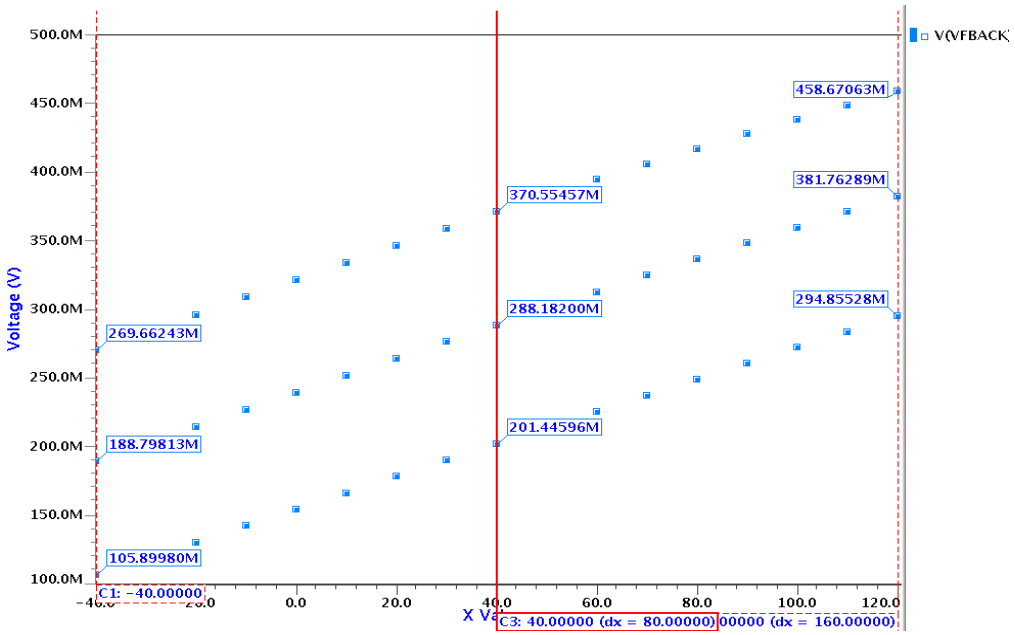

Figure 19 Vfback node variation w.r.t. temperature for TYP, MIN and MAX corners

The Vfback node is plotted, as shown in Fig. 19, for all three process corner over temperature and it was observed that the minimum to maximum range of Vfback node is 105.8mV to 458.6mV.

c. I_1 and I_2 are divided into I_{1a}, I_{1b} and I_{2a} and I_{2b}. Division of current is done by using resistors at both the V_{in1} and V_{in2} nodes. The voltage at nodes V_{in1} and V_{in2} is made equal, for that equal resistor value is used such that $I_{1a} = I_{2a}$ and $I_{1b} = I_{2b}$.

The operational amplifier is used to make the V_a and V_b node equal. Form KCL,

$$V_{in1} = I_{1b}R_1 = V_{in2} = I_{2b}R_2 \qquad 3.10$$

Therefore,

$$I_{2a} = \frac{V_{in1}}{R_2} = \frac{V_{GS1}}{R_2} \ (V_{in1} = V_{GS1}) \qquad 3.11$$

From branch 2,

$$V_{in2} = V_{GS2} + I_{2b}R_1 \qquad 3.12$$

As, $V_{in1} = V_{in2}$, equation can be written as

$$V_{in1} = V_{GS2} + I_{2b}\mathrm{R}_1 \quad 3.13$$

Replacing V_a with V_{GS1}

$$V_{GS1} = V_{GS2} + I_{2b}\mathrm{R}_1 \quad 3.14$$

$$V_{GS1} - V_{GS2} = I_{2b}\mathrm{R}_1 \quad 3.15$$

$$\Delta V_{GS} = I_{2b}\mathrm{R}_1 \quad 3.16$$

$$I_{2b} = \frac{\Delta V_{GS}}{\mathrm{R}_1} \quad 3.17$$

For the reference voltage, I_2 is replicated in the 3rd branch,

$$V_{out} = I_3\mathrm{R}_4 = I_2\mathrm{R}_4 \quad 3.18$$

I_2 is summation of I_{2a} and I_{2b}

$$V_{out} = (I_{2a} + I_{2b})\mathrm{R}_4 \quad 3.19$$

$$V_{out} = (\frac{V_{GS1}}{R_2} + \frac{\Delta V_{GS}}{\mathrm{R}_1})\mathrm{R}_4 \quad 3.20$$

The V_{ref} obtained is summation of the PTAT and CTAT currents. Term $\frac{V_{GS1}}{R_2}$ is responsible for PTAT and $\frac{\Delta V_{GS}}{\mathrm{R}_1}$ for CTAT. Proper values of R_1 and R_2 will compensate the PTAT and CTAT components resulting a temperature independent voltage. R_4 is used to define the value of reference output voltage required.

d. The conventional 5T operational amplifier at such low supply voltage doesn't met the bias margins for proper functioning. Thus a new design is implemented in which the tail current source is removed, as shown in Fig 20. This could affect the common mode rejection ratio. But as it is operated in the subthreshold region the gain achieved is high. The input pair, NMOS are matched with the diode connected NMOS used in BGR core.

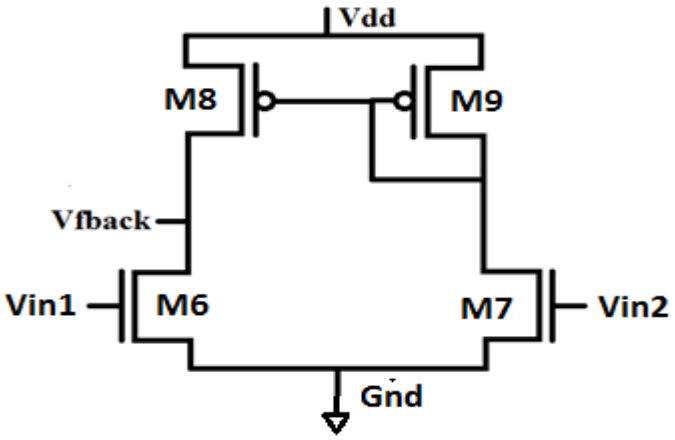

Figure 20 Proposed 4T Operational Amplifier (single stage)

Thus input pair also works in subthreshold region. The current source of Opamp are also matched with the PMOS used in BGR core for mirroring current, Such that the Vfback voltage, the output of Opamp is obtained to bias the PMOS mirrors of BGR.

The variation of input voltage of Opamp is plotted across the temperature range of -40°C to 120°C, plotted in Fig. 21. It is observed that the input offset error was maximum seen at the MAX corner at 120°C.

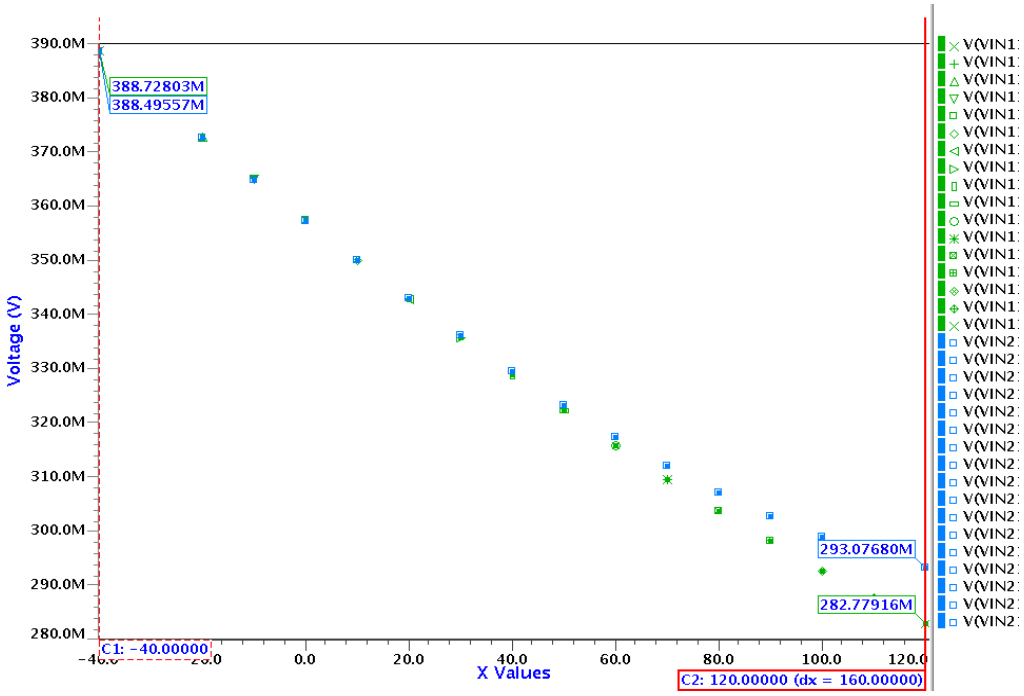

Figure 21 Variation of Vin1 and Vin2 w.r.t. temperature, the offset error.

e. Startup circuit design as described in section 3.2.1 is not used as the trip point at which invertor should flip is not achieved. Thus in this case an ideal pulse of 5ns is applied via NMOS to provide an initial trigger to the BGR circuit. The NMOS is connected to Vfback node as shown in Fig 22.

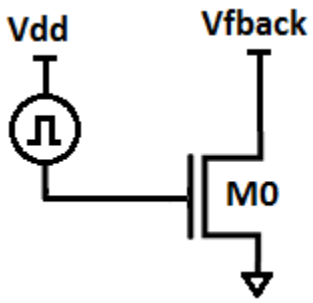

Figure 22 Setup to give a Startup trigger

The transient response so observed in Fig. 23 is simulated for TYP corner at 27°C. At 10µs the enable signal is asserted and it is observed that almost after 463µs the desired value of Vout has been achieved.

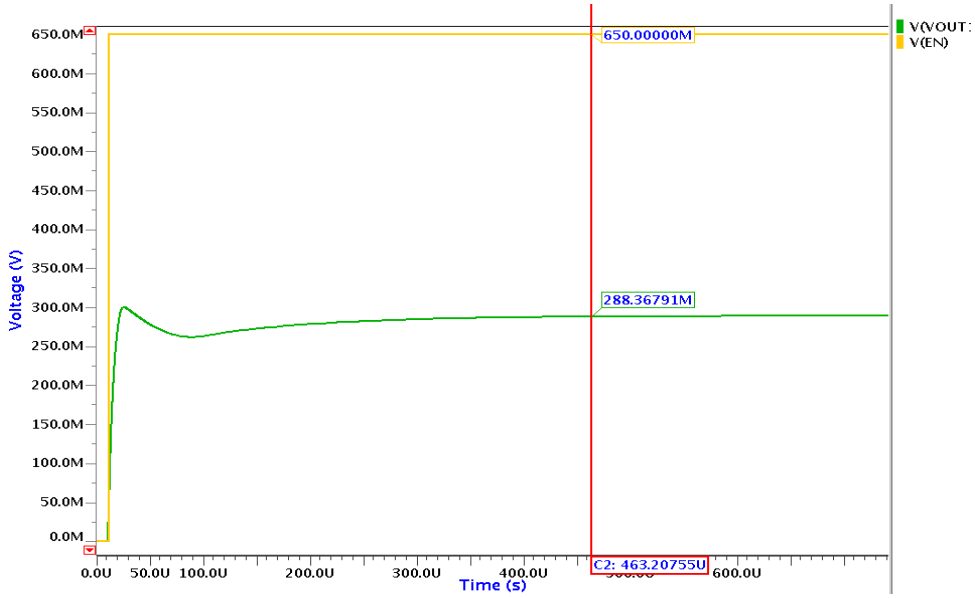

Figure 23 Transient profile of the Vout node after the trigger is applied

3.3 Results

3.3.1 Simulated results at 950mV supply voltage

The proposed design is simulated over three process corners namely MIN, TYP and MAX. The swept temperature rang is -40°C to 120°C. Various node voltages and current of branches are measured and tabulated below.

Table 5 Various parameters at all 3 corners for voltage mode BGR at 950mV supply voltage

Parameters/corner	MIN	TYP	MAX
VOUT	782.5mV-786mV	705mV- 713mV	626.5mV-634mV
R2	207.2k-228kOhm	308k-327kOhm	461.2k-471.6kOhm
I_{out}	1.1uA-1.43uA	764nA-1.04uA	538.3nA-768.4nA
R1	149.6k-164.7kOhm	207k-221kOhm	279.8k-286.1kOhm
I2	570nA-758.5nA	391.8nA-538.4nA	275.7nA-395.5nA
VIN1	502.4mV-389.6mV	418.1mV-298.1mV	336.6mV-210.9mV
VIN2	501.37mV-389.5mV	417.7mV-297.6mV	336.2mV-209.6mV
Vfback	286.5mV-392.6mV	385.1mV-506.6mV	477.1mV-611.4mV

The DC, Monte Carlo simulations results are compiled below:

a. DC Simulations

- At TYP process corner

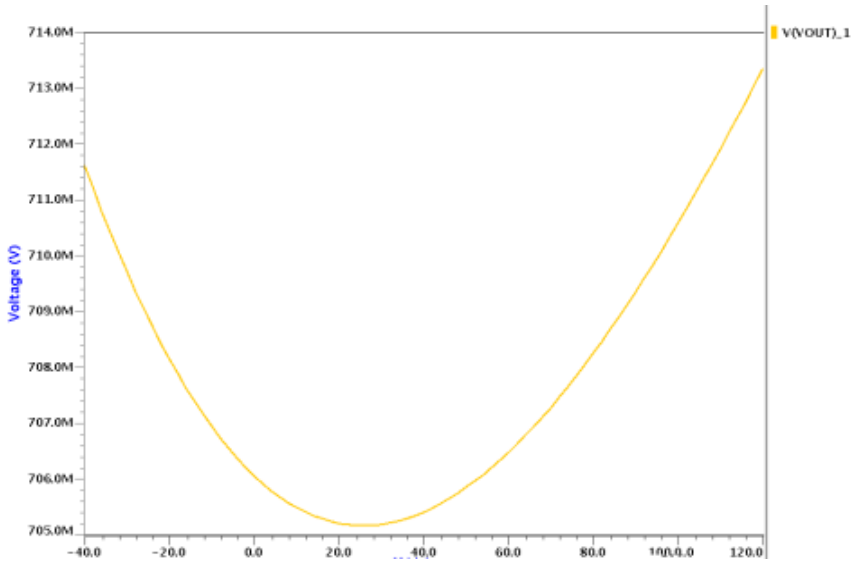

Figure 24 DC simulation result at TYP corner before and after trimming

Reference voltage is 700mV.
After trimming: Variation across -40°C to 120 °C is 705mV- 713mV

- At MIN process corner

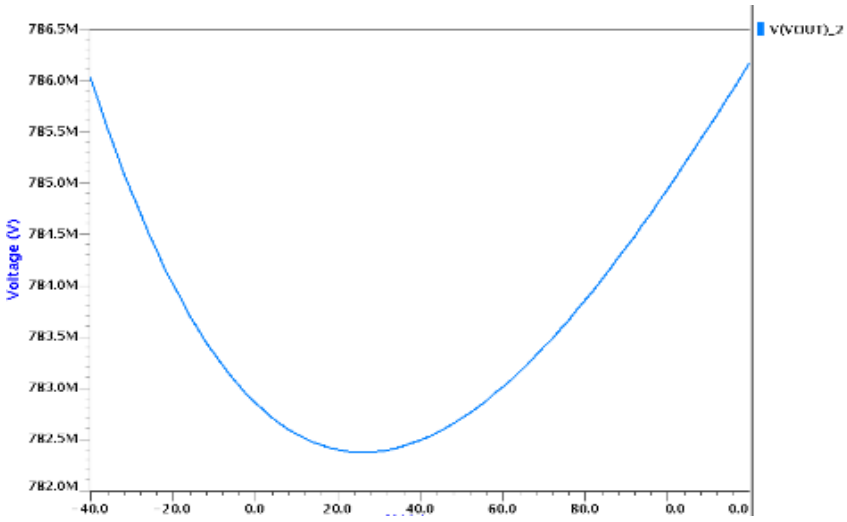

Figure 25 DC simulation result at MIN corner before and after trimming

After trimming: Variation across -40°C to 120 °C is 782.5mV-786mV

- At MAX process corner

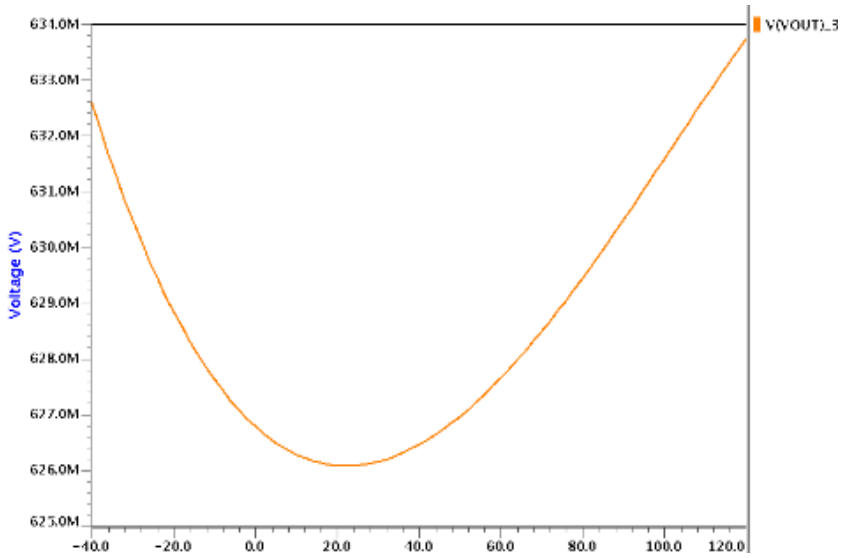

Figure 26 DC simulation result at MAX corner after trimming

After trimming: Variation across -40^{o}C to 120 ^{o}C is 626.5mV-634mV

Only voltage mode trimming is done to get the best compensated slope for CTAT and PTAT variations. With only single trimming mode, either current trimming or voltage trimming, the desired value of output BGR is not achieved. That's why the reference at every corner is settled at different value. To set the final output voltage to a specific voltage level for every process corner, provision of current trimming have to present in the circuit. This unnecessarily increases the circuit area. An alternate is to use the current mode architecture.

b. Monte Carlo Simulations (Iteration number =2000)
   - At TYP process corner: Coefficient of variation: 5.21%

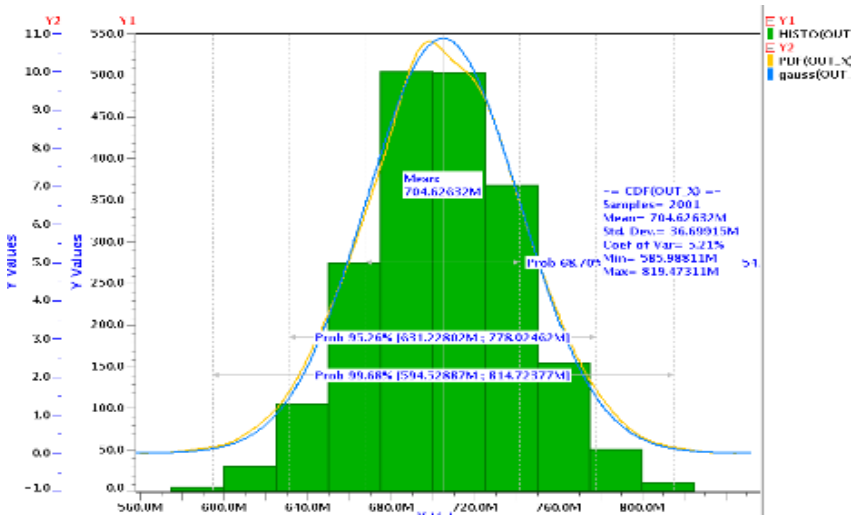

Figure 27 MC simulation output histogram at TYP corner after trimming

- At MIN process corner: Coefficient of variation: 3.21%

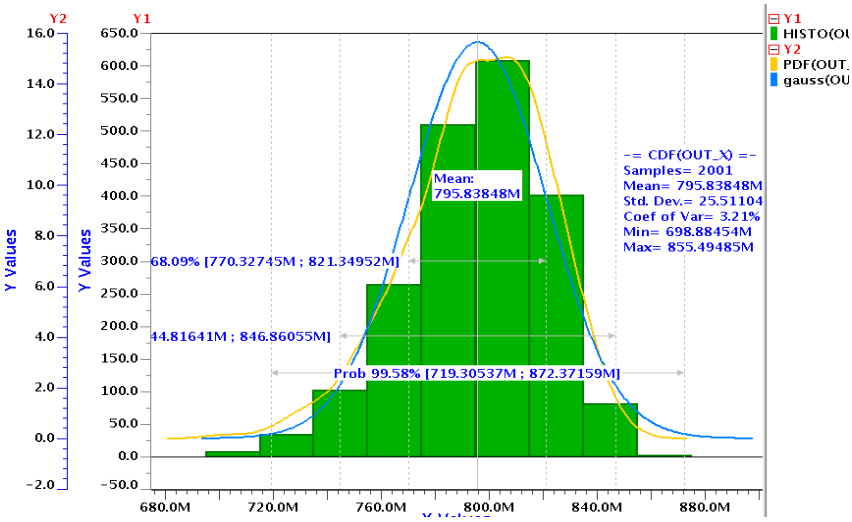

Figure 28 MC simulation output histogram at MIN corner after trimming

- At MAX process corner: Coefficient of variation: 6.74%

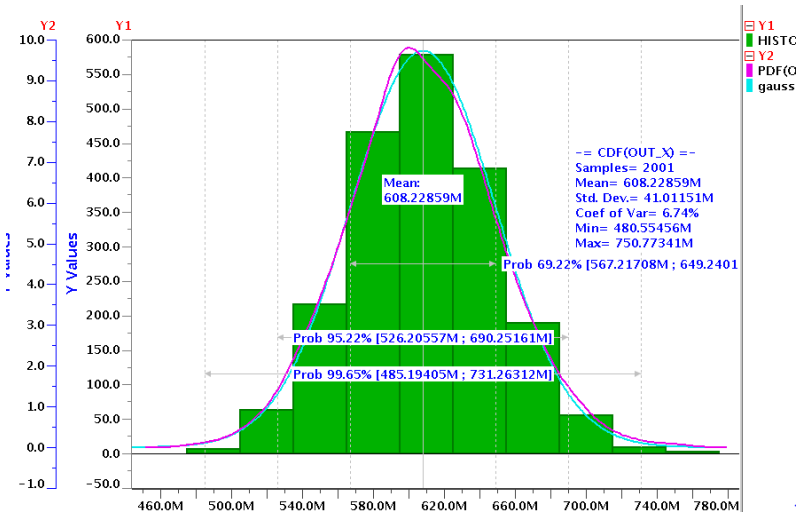

Figure 29 MC simulation output histogram at MAX corner before and after trimming

The temperature coefficient after trimming is 50ppm/^{o}C. Also the coefficient of variation is 5%. Finally the current mode architecture is explored, which includes only voltage trimming. The results of BGR with 650mV supply voltage are quoted in section 3.3.2.

3.3.2 Simulated results at 650mV supply voltage

For the proposed design all the parameters across all the three corners are tabulated below.

Table 6 Various parameters at all 3 corners for voltage mode BGR at 650mV supply voltage

Parameters/corner	MIN	TYP	MAX
V_{OUT}	248.4mV-251.5 mV	249.4mV-255.0mV	248.3mV-261mV
$R_1(n)$	1.55MOhm	1.55MOhm(140)	1.55MOhm
I_1	211.0nA-193.8nA	142.8nA-135.2nA	120.6nA-118.9nA
I_{1a}	70.4 nA -94.4 nA	50.7nA-72.9nA	37.9nA- 63.8nA
I_{1b}	140.6 nA -99.2nA	91.5nA-61.6nA	82.7nA -52.7nA
$R_2(n)$	4.5MOhm(405)	4.34MOhm(390)	3MOhm(270)
I_{out}	211.0nA-193.8nA	142.8nA-135.2nA	120.6nA-118.9nA
Pout	514nW-526nW	352.6nW-388.5nW	324.8nW-356.6nW
$R_3(n)$	1.6MOhm(144)	1.82MOhm(164)	1.72MOhm(155)
V_{IN1}	467.9mV-361.0mV	388.71mV-277.3mV	311mV-202.2mV
V_{IN2}	467.4mV-361.5mV	388.47mV-280.2mV	310.8mV-212.5mV
V_{fback}	106.9mV-296.6mV	188.8mV-384.9mV	261.9mV-459.2mV

The DC, Monte Carlo and AC simulation results compiled below are after trimming is applied.

a. DC Simulations
   - At TYP process corner

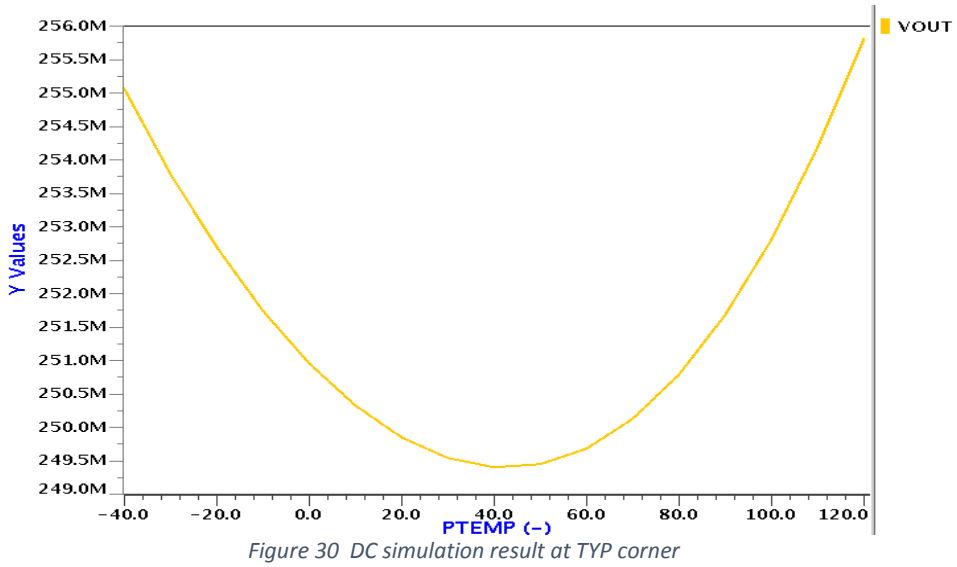

Figure 30 DC simulation result at TYP corner

Variation across -40°C to 120 °C is 249.4mV-255.0mV.

- At MIN process corner

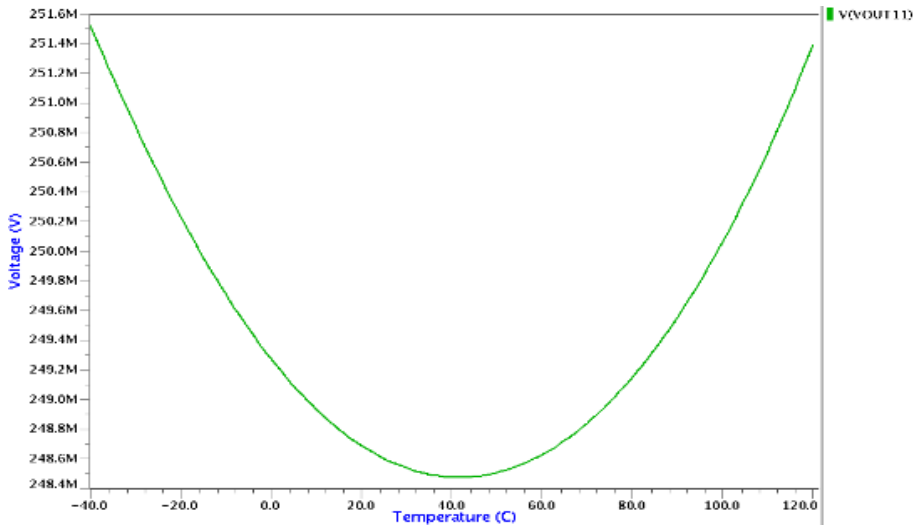

Figure 31 DC simulation waveform at MIN corner

Variation across -40^{o}C to 120 ^{o}C is 248.4mV-251.5 mV.

- At MAX process corner

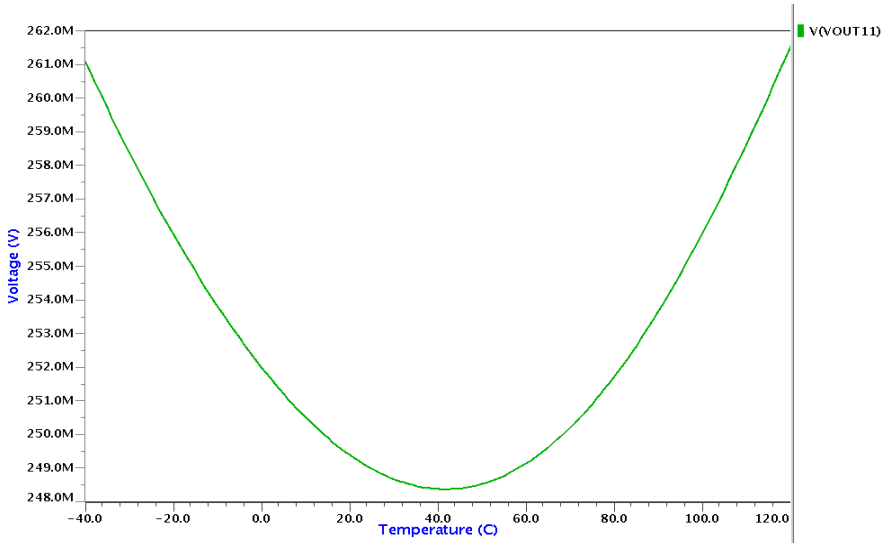

Figure 32 DC simulation waveform at MAX corner

Variation across -40^{o}C to 120 ^{o}C is 248.3mV-261mV

b. Monte Carlo Simulations (Iteration number =2000)

- At TYP process corner: Coefficient of variation: 2.81%

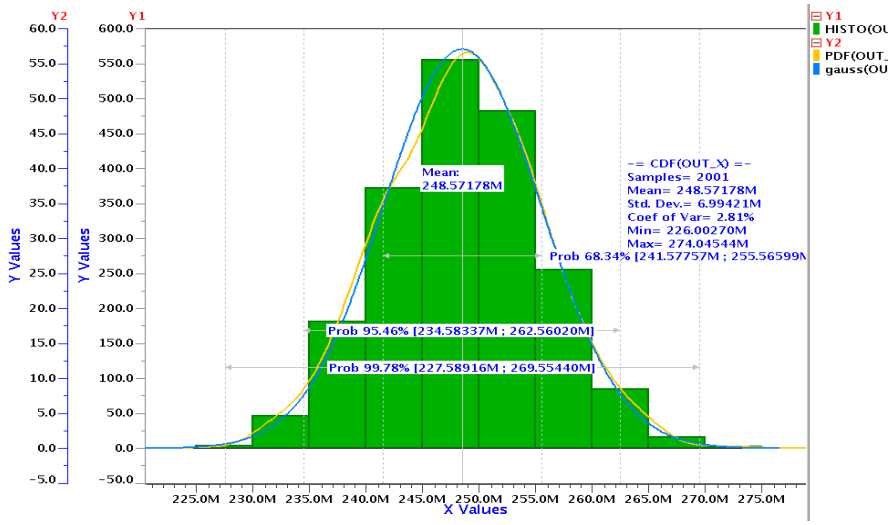

Figure 33 MC simulation output histogram at TYP corner

- At MIN process corner: Coefficient of variation: 3.04%

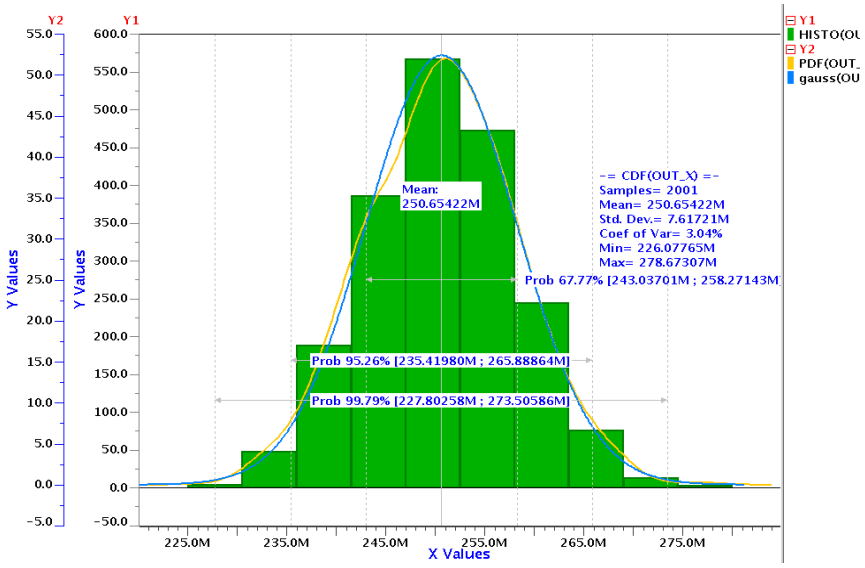

Figure 34 MC simulation output histogram at MIN corner

- At MAX process corner: Coefficient of variation: 2.93%

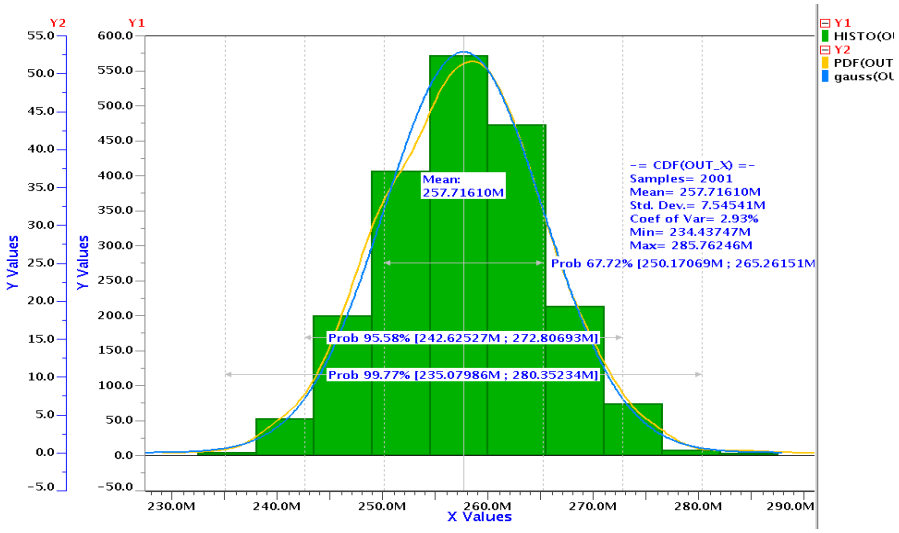

Figure 35 MC simulation output histogram at MAX corner

From the .chi file the result of sensitivity was extracted for TYP, MIN and MAX corners. It is observed that the maximum contribution for deviation of mean value, about 28% of the total, is caused by the current mirrors i.e. the PMOS current mirror of the BGR core. Thus for minimizing the variation the size can be increased but the size should be optimized. Second major contributors, of almost 15%, are diode connected NMOS and the input pair of the Opamp.

The standard deviation across TYP MIN and MAX corners are 6.99mV, 7.61mV and 7.54mV respectively at 27^{o}C temperature.

c. AC simulation

AC analysis is done on 3 temperature samples i.e. -40°C, 30°C and 120°C. The loop is broken at the V_{fback} node so that the combined effect of negative closed loop and positive loop is observed.

For the three process corners the gain and phase plot are observed as shown in Fig. 36, 37 and 38.

- At TYP process corner

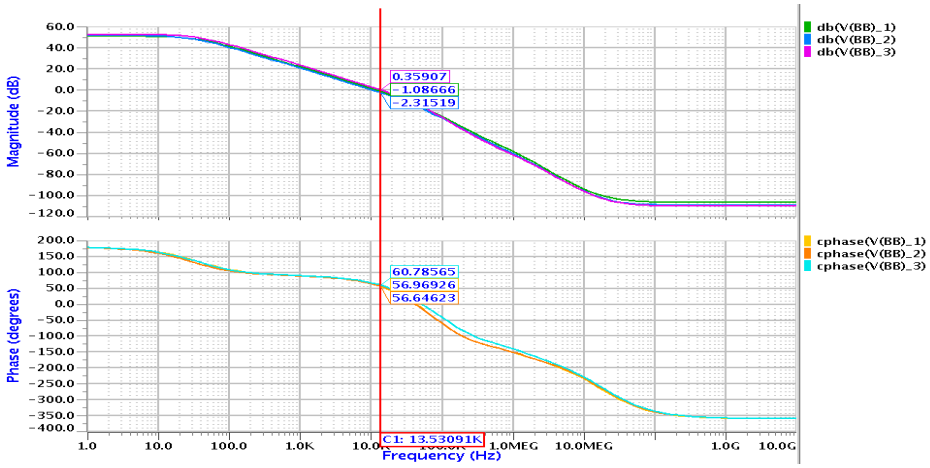

Figure 36 Gain and Phase plot of OPAMP for TYP corner

Gain: 52dB ; Phase margin: 58°

- At MIN process corner

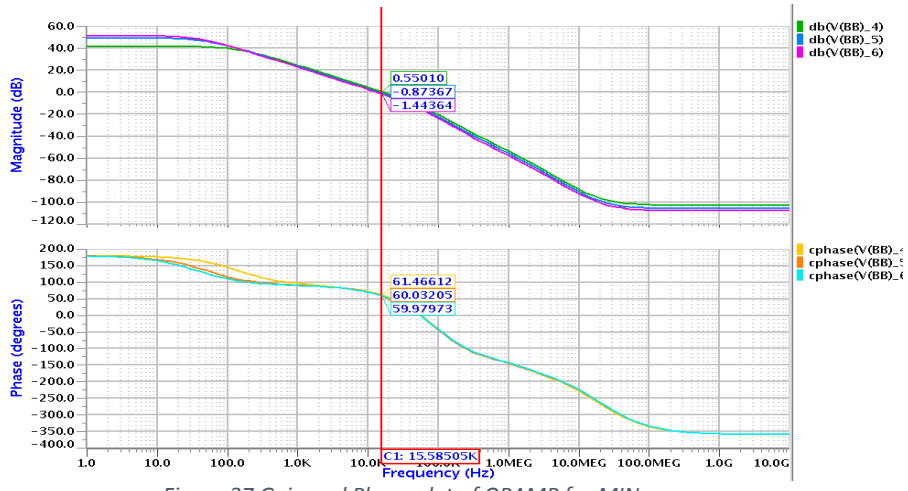

Figure 37 Gain and Phase plot of OPAMP for MIN corner

Gain: 41dB ; Phase margin: 60°

- At MAX process corner

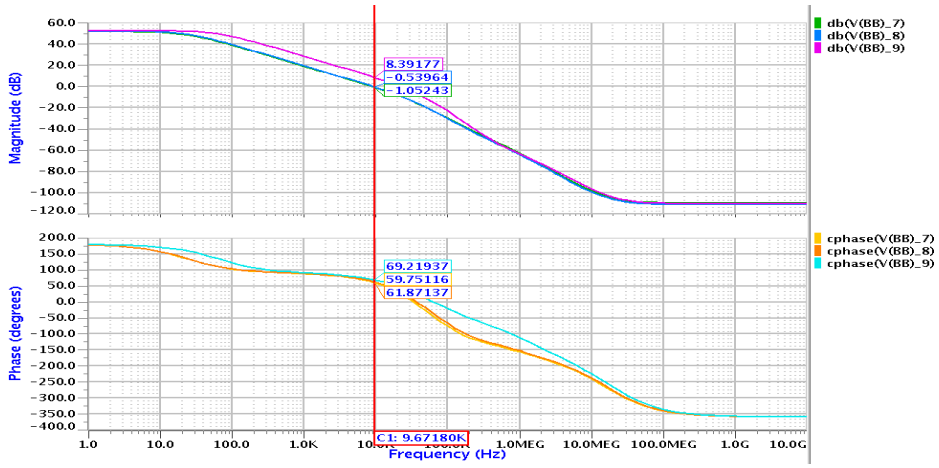

Figure 38 Gain and Phase plot of OPAMP for MAX corner

Gain: 52dB ; Phase margin: 63^{o}

It was observed that the gain so obtained in subthreshold region of operation of Opamp is sufficient enough to minimize the offset error. As the offset error is less the variation in output voltage is seen less.

Further the phase margin so observed was sufficient to make the closed loop Opamp stable.

Chapter 4

Conclusion and Future Work

4.1 Conclusion

The PVT compensated Bandgap reference is implemented in BCD9s (110nm) technology. Two designs are proposed one in voltage mode with a supply voltage of 950mV, with a reference voltage of 700mV and another in current mode with a supply voltage of 650mV, having reference voltage of 250mV. The temperature coefficient, over the range of -40^{o}C to 120^{o}C of the designed bandgap reference at 950mV and 650mV supply is 50 ppm/^{o}C and 35ppm/^{o}C respectively.

For BGR at 950mV:
The temperature coefficient achieved is less i.e. 50ppm/^{o}C. The coefficient of variation observed, after Monte Carlo simulation for 2000 samples, is $\pm$6% in worst case. This design was not aligned with the state of art because the power consumption was very high, additionally area overhead is there because of utilization of both current and voltage mode of trimming. So further, design was implemented at 650mV supply voltage. Voltage mode is not supported well at 650mV supply voltage design so it was implemented in current mode.

For BGR at 650mV:
As compared to other designs the proposed design is competitive in terms of that, with weighted V_{GS} technique, the temperature coefficient achieved is very less i.e. 35ppm/^{o}C. The coefficient of variation observed, after Monte Carlo simulation for 2000 samples, is $\pm$3% in worst case. The static power consumption is typically 364nW, while the worst case is 526.5nW (MIN corner). It will serve well for the ultra-low power applications. No charge pump is used to boost up the supply voltage for proper working of the core cell as use in [1] and [3]. The table 7 shows the comparison between this work and recent work done in domain of subthreshold BGRs.

4.1.1 Comparison table

The results of the implemented design are analyzed and compared with the various designs which have been proposed in past couple of years.

Table 7 Comparison of proposed design with present state of art

Parameters	Proposed	Ref [1]	Ref [2]	Ref [3]	Ref [4]	Ref [5]	Ref [6]
Year	2018	2017*	2015*	2015*	2013*	2011*	2011
Supply voltage	650mV	500mV	950mV	500mV	700mV	750mV	840mV
Temperature range(°C)	-40 to 120	-40 to 120	-40 to 105	0 to 80	-40 to 120	-20 to 85	27-125
Operation current	560nA	110nA	10.1uA	-	-	226nA	2.2uA
Transistor ratio	8	8	10	-	-	50	100
Reference voltage	250mV	370mV	750mV	500mV	548mV	250mV	325mV
Temperature coefficient(ppm/°C)	35	8	131	75	114	40	59
Power consumption	364nW	55nW	9.5uW	32nW	53nW	170nW	1.8uW
Technology used	BCD9s 110nm	CMOS 40nm	CMOS 180nm	CMOS 130nm	CMOS 180nm	CMOS 130nm	_

*marked are the measured results while rest other are simulated ones.

The proposed work is done on BCD technology platform while rest other cited papers are in CMOS technology. Hence comparing the parameters one to one will not yield the best picture.

In comparison to [1], [3] the results so obtained with the design proposed in this thesis work, at architecture level, are not up to the expectation such as power consumption and temperature coefficient. But the key point to observe is that both the designs in [1] and [3] have used an additional charge pump to boost up the supply voltage of the BGR core. While the proposed design solely works at 650mV well in the bias margins.

In [1] and [3], BJTs are used as CTAT voltage generation while the proposed design utilized NMOS. Also BGR is duty cycled to decrease the power consumption in [1]. But this decrement in power consumption is at the cost of output ripple, while the 364nW power consumption in proposed design is the static power. The power consumption can further be reduced, but in BCD9s, after simulations it is observed that the I_{OFF} is around 6nA. Thus to have a reliable design the operating current is kept 10 times greater than the leakage current.

The proposed design covers a wide range of temperature i.e. -40°C to 120°C which makes it more reliable.

Various designs such as [5] and [6] have used transistor ratio of 50 and 100 respectively. Trial simulations are done with the increased transistor ratio, but it is observed that V_{GS} at MAX corner decreases very much that it no longer works in subthreshold, rather tends to be in cutoff. Thus transistor ratio of 8 is optimized ratio for this work.

4.2 Future Work

Due to the extreme low amount of current usage the time taken to get the stabilized result is comparatively more i.e. in range of hundreds of Micro-seconds. To cater this trade off various design alterations can be done to improve the settling time with low power consumption.

An alternate, in place of large resistors can be implemented to save the area. The layout of design can be implemented and further results can be validated.

The design can be explored with other technologies for better results such as FDSOI(28nm) or with emerging BCD10 technology (90nm).

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